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FORMATION OF SOURCE/DRAIN FROM DOPED GLASS

Abstract:

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(71) Applicant *(for all designated States except US)*: INTEL CORPORATION [US/US]; 2200 Mission College Boulevard, Santa Clara, CA 95052 (US).

(72) Inventors; and
(75) Inventors/Applicants *(for US only)*: THOMPSON, Scott, E. [US/US]; 19635 N.W. Rock Creek Way, Portland, OR 97229 (US). JAN, Chia-Hong [US/US]; 5200 N.E. Elam Young Parkway, Hillsboro, OR 97124 (US). PACKAN, Paul, A. [CA/US]; 15025 S.W. Gibraltar Court, Beaverton, OR 97007 (US). GHANI, Tahir [US/US]; 5200 N.E. Elam Young Parkway, Hillsboro, OR 97124 (US). ANDIDEH, Ebrahim [US/US]; 5200 N.E. Elam Young Parkway, Hillsboro, OR 97124 (US). MOGHADAM, Farhad, K. [US/US]; 5200 N.E. Elam Young Parkway, Hillsboro, OR 97124 (US). BOHR, Mark, T. [US/US]; 19475 S.W. Suncrest, Aloha, OR 97007 (US).

(74) Agents: TAYLOR, Edwin, H. et al.; Blakely, Sokoloff, Taylor & Zafman, Seventh floor, 12400 Wilshire Boulevard, Los Angeles, CA 90025-1026 (US).

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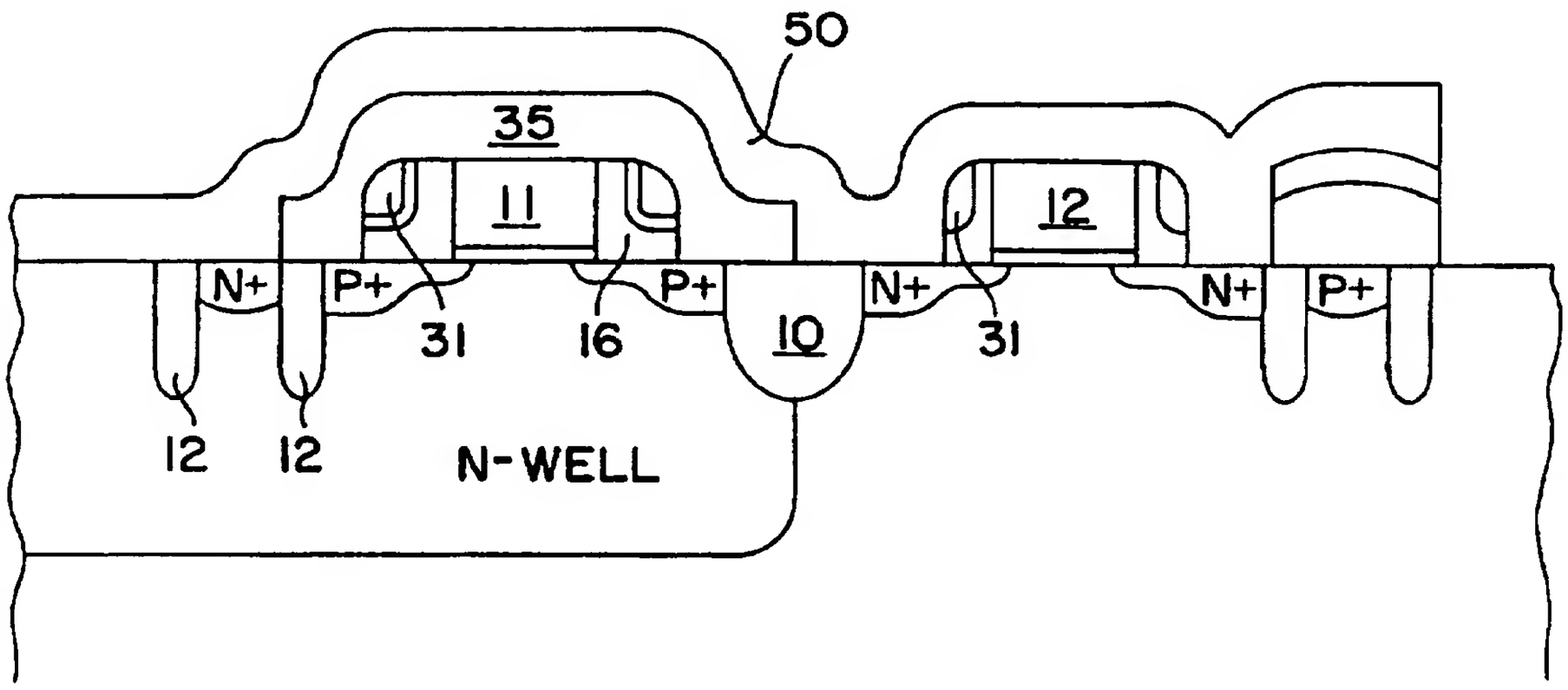

(57) Abstract

A process for fabricating a source and drain region which includes a more lightly doped source and drain tip region immediately adjacent to the gate and a more heavily doped main portion of the source and drain region spaced apart from the gate. A first layer (16) of glass (2 % BSG) is used to provide the source of doping for the tip region and a second layer (35) of glass (6 % BSG) is used to provide the dopant for the more heavily doped major portion of source and drain regions. Spacers (31) are formed between the glass layers to define the tip region from the main portion of the source and drain regions.

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--FORMATION OF SOURCE/DRAIN FROM DOPED GLASS--

1. Field of the Invention

The invention relates to the field of forming self-aligned source and drain regions for field-effect transistors.

2. Prior Art

Typically during the formation of a field-effect transistor, ion implantation is used to align a source and drain region with a gate (and/or with gate spacers in some processes). The ion implantation damages the crystalline structure of the silicon substrate necessitating thermal annealing. During the annealing the implanted dopant diffuses thereby deepening the source and drain regions. These deeper regions make it difficult to control the adverse effects of short channels. Ideally, to control the short channel effects where effective channel lengths are in the order of 0.1um or less, the source and drain extension regions should be extremely shallow and heavily doped (e.g., 0.05 to 0.1um versus 0.2 to 0.4 um for 0.2 to 0.5 um channel length transistors).

Scaling implanted p+ junctions is particularly difficult since the light boron (B^{11}) ions channel during implantation and secondly, since the ions damage the silicon bonds causing point defects. These point defects significantly increase the diffusion of the boron atoms (up to 1000 times) during subsequent thermal annealing. Thus, even for light ions, such as B11, and low energy implants, the implant damage results in enhanced diffusion.

One solution to this problem is to make amorphous the silicon substrate before the B11 implant since this reduces channeling. However, the net result is not a significantly shallow profile since the damage to the silicon lattice leads to enhance diffusion of the implanted B11.

Another technique for solving this problem is to diffuse the portion of the source and drain regions adjacent to the gate (tip or tip region) from doped spacers and to form the more heavily doped main portions of the source and drain regions by ion implantation. This provides some

advantage over the ion implantation of both the tip region and main portion of the source and drain regions but implant damage from the source/drain implant still affects the depth of the diffused tip region resulting in degraded short channel effects. Short channel effects are discussed in numerous publications such as Silicon Processing for the VLSI Era, Vol. 2, by S. Wolf, published by Lattice press, see Section 5.5, beginning at page 338.

As will be seen, the present invention permits the simultaneous formation of both an ultra shallow heavily doped source and drain extension region, main portions of the source and drain regions and doping of the polysilicon gate without ion implantation.

SUMMARY OF THE INVENTION

A method is described for fabricating field-effect transistors on a substrate where the source and drain regions are formed in alignment with a gate. A source of dopant is used having (i) a more lightly doped region which is formed directly adjacent to the gate and (ii) a more heavily doped region spaced apart from the gate. This dopant source is formed on the surface of the substrate. The dopant is diffused from the source of dopant in a heating step simultaneously forming both the lightly doped source and drain tip region and the main portion of the source and drain regions. This diffusion is done in an ambient that may include oxygen or ammonia.

In one embodiment boron is diffused from two different layers of borosilicate glass (BSG). Spacers are formed adjacent to the gate by anisotropically etching a silicon nitride layer which overlies a 2% BSG layer. Then a 6% BSG layer is formed over the spacers and 2% BSG layer to supply the dopant for the more heavily doped main portion of the source and drain regions. Both BSG layers are annealed prior to being patterned to prevent the formation of an unstable boron compound that would otherwise adversely effect diffusion. Rapid thermal processing is used to diffuse the dopant into the substrate from both BSG layers.

In one embodiment the substrate surface is first damaged by a heavy neutral species such as silicon or implanted with a neutral species

such as carbon which can be used to increase or decrease the diffusion of boron in the substrate before the doped glass is deposited on the substrate. In another embodiment a chemically formed oxide of 5-20Å is formed over the substrate prior to formation of the doped glass. These techniques can be used to decrease or increase the depth of the later formed source and drain regions for a given anneal time and temperature.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a cross sectional elevation view of a section of a substrate showing an n-well isolated from a p-well. Polysilicon gates and a first glass layer are also shown.

Figure 2 illustrates the substrate of Figure 1 after a first photoresist layer has been masked and etching, and during an ion implantation step used to form the tip regions for the n-channel transistor.

Figure 3 illustrates the substrate of Figure 2 after the formation of a TEOS layer and a silicon nitride layer.

Figure 4 illustrates the substrate of Figure 3 after the silicon nitride layer has been anisotropically etched to form spacers and after the substrate has been covered with a second glass layer.

Figure 5 illustrates the substrate of Figure 4 after the masking and etching of a photoresist layer and during an ion implantation step used to form the main portion of the source and drain regions for the n-channel transistor.

Figure 6 illustrates the substrate of Figure 5 after diffusion of the boron dopant from the glass layers to form the source and drain regions for the p-channel transistor.

Figure 7 illustrates the substrate of Figure 4 for an alternate embodiment where the n-type dopant is diffused from a glass layer.

Figure 8 illustrates a preliminary processing step for the substrate of Figure 1 prior to the formation of the first glass layer.

Figure 9 illustrates another preliminary step for the substrate of Figure 1 prior to the formation of the first glass layer.

DETAILED DESCRIPTION OF THE INVENTION

A method and structure for forming low damage, shallow source and drain regions in alignment with a gate for a field-effect transistor is described. In the following description, numerous well-known steps such as masking and etching steps are not discussed in detail in order not to obscure the present invention. In other instances, specific details are set forth such as specific boron dopant concentrations in order to provide a thorough understanding of the present invention.

The various layers of materials shown in the drawings are not shown to scale. Rather, the layers have been made clearly visible so that the present invention can be better understood from the drawings. Additionally, only a portion of a substrate showing a single p-channel and n-channel transistor is illustrated. It will be appreciated that in practice the invention is used to fabricate an entire integrated circuit.

While the present invention is not limited to any particular geometry in one embodiment, it is used for the fabrication of transistors having a channel length of approximately 0.1um with transistors that operate from a 1.8 volt supply.

Referring now to Figure 1, a section of a monocrystalline silicon substrate 15 is illustrated having a well doped within an n-type conductivity dopant (n well 21) and a region or well doped with a p-type conductivity dopant (p well). As will be seen, it is not important to the present invention whether both n and p wells are used. For instance, an n well may be used for p-channel transistors with the n-channel transistors being formed directly in a p-type substrate.

The n and p well of Figure 1 are isolated from one another by a recessed isolation region specifically, trench 10. Additionally, within the n well 21 there are other isolation trenches 12 for isolating from one another p-channel transistors formed within the n well. Likewise, there are isolation trenches 13 formed within the p well to isolate n-channel transistors formed in the p well from one another. The isolation trenches may be formed using well-known technology. Other isolation technologies such as local oxidation of silicon (LOCOS) may be used instead of trenches

A gate insulative layer (such as a high quality, thermally grown oxide to insulate the gate from the substrate) is formed over the substrate. Following this, a polycrystalline silicon (polysilicon) layer is deposited and the gates for the field-effect transistors are fabricated using ordinary photolithographic and etching techniques. Two such gates insulated from the substrate are shown in Figure 1. Gate 11, formed above the n well, as will be seen, is used for a p-channel transistor; the other gate 14, formed above the p well, is used for an n-channel transistor. Numerous steps typically used before the fabrication of the gates are not illustrated, such as cleaning steps, ion implantation steps to adjust threshold voltage, etc. Additionally, other processing steps for reducing the amount of diffusion are discussed later in conjunction with Figures 8 and 9.

Following the formation of the gates 11 and 14 a conformal layer 16 of borosilicate glass (BSG) is deposited over the entire substrate. This layer may be 100Å-300Å thick. The layer in one embodiment has a 2% functional description concentration of a p-type conductivity dopant (boron). This layer is referred to hereinafter as 2% BSG layer. TEOS or silane based chemistry is used to deposit the 2% BSG layer. This layer is formed in one embodiment at a temperature of 400-600°C.

It has been determined that more uniform diffusion occurs if the BSG layer 16 is densified prior to patterning. Unless this occurs, water from the photoresist can react with B_2O_{3+x} in this glass leaving an unstable B_2O_{3-x}. By annealing this layer prior to contact with the photoresist, a stable boric acid is formed and this results in a better diffusion source. This annealing is done at a relatively low temperature (650°C to 800°C). A rapid thermal annealing (RTA) is used in one embodiment having a 15 second ramp up - 20 second steady state and 15 second ramp down.

In the embodiment of the present invention described in this application, the p-channel transistor is formed using the present invention while the n-channel transistor is formed using well-known ion implantation. The formation of the n-channel transistor is described

nonetheless since the masking steps for the n-type implants are used to diffuse the p-type dopant sources.

Figure 2 illustrates the first of two ion implantation step used in the formation of the n-channel transistor. First, a photoresist layer 17 is formed over the substrate 15. This layer is masked exposed and developed by well-known techniques to reveal the substrate regions where the source and drains are formed for the n-channel transistors and additionally, regions where an n-type dopant is used for well tap 20. This is shown in Figure 2 where the photoresist members 17 protect predetermined areas of the substrate while leaving exposed other areas. Next, the exposed portions of glass layer 16 are etched in alignment with the photoresist members 17. This etching step uses a hydrogen fluoride (HF) based solution. The substrate is then subjected to ion implantation of an arsenic dopant as shown by the arrows 18. This forms the regions 19 in alignment with the gate 14 and a region 20 between the trenches 12. This arsenic doping implant is relatively light and is used for forming the tip regions of the source and drain regions for the n-channel transistor. The main portions of the source and drain regions for this n-channel transistor are subsequently formed with the second ion implantation step.

Next, as shown in Figure 3, a conformal layer of undoped silicon dioxide is formed from tetraethyl orthosilicate (TEOS) by low pressure chemical vapor deposition layer 30 or other undoped LPCVD oxide film is formed over the substrate using well-known processing. This layer provides an etchant stop for the spacers formed for the n-channel transistor. The TEOS layer may be 50Å-300Å thick.

Now, as shown in Figure 3 a conformal layer 31 of silicon nitride is formed over the TEOS layer 30. (An oxide layer may be used instead of the silicon nitride layer.) This silicon nitride layer is approximately 800Å thick in one embodiment. Well-known type, i.e., sufficient selectively anisotropic etching is used to etch the silicon nitride layer to form spacers 31 shown on opposite sides of gates 11 and 14 of Figure 4. The TEOS layer acts as an etchant step to protect the silicon. The TEOS and BSG

regions not covered by the nitride spacers are then etched away. A wet etchant may be used for this purpose.

A thin layer of silicon dioxide (5-20Å of chemically grown oxide) may now be formed so that there is an ultra thin uniform oxide on the exposed silicon prior to formation of the second glass layer. The purpose of this oxide is discussed in conjunction with Figure 8.

Following this, a second layer 35 of BSG is formed over the substrate. This time, however, the layer has a 6% concentration of boron (6% BSG). This layer in one embodiment is approximately 200Å-600Å thick and is deposited using a TEOS or silane based chemistries at a temperature of 400-600°C in one embodiment.

This second glass layer is annealed prior to patterning in an RTA step in the same manner and for the same reason as the first glass layer as discussed above.

As shown in Figure 5, following the formation of the 6% BSG layer 35 and its annealing, a photoresist layer 40 is masked, exposed and developed to expose generally the same areas that were exposed in Figure 2. Specifically, gate 12, the areas adjacent to gate 12 (source and drain regions) and region 20; the remainder of the substrate shown in Figure 5 is protected by the photoresist members 40.

The cap layer over the glass layer 35 (if used) and the 6% BSG layer 35 are then etched in alignment with the photoresist members 40. This is done by HF based chemistry.

The second n-type ion implantation step is now used to implant the arsenic dopant into the regions of the substrate not protected by the photoresist layer 40, spacers 31, or gate 12. The arrows 41 illustrate the implantation of this arsenic dopant. This dopant is used to form the main portions N+ of the 45 source and drain regions for the n-channel transistors. Note that since the spacers 31 are in place, the dopant is implanted in alignment with the spacers and not in alignment with the gate.

Following this, a driving (heating) step, is used. The p-type dopant from the 2% BSG and 6% BSG layers is simultaneously diffused into the substrate to form both the tip regions, main source and drain regions, and

doping of the gate 11 for the p-channel transistor. The tip region has a depth of 300-700Å which the main portion of the p-type region has depth of 1000-2500Å. Additionally, the p-type dopant from the BSG layers forms a well tap between the isolation trenches 13. In one embodiment, this drive step employs rapid thermal processing. Specifically, driving at 1000°C to 1040°C for 10-20 seconds with ramping up to and down from this temperature at 70°C per second. A standard Halogen lamp band rapid thermal reactor is used.

The depth of these regions can be made even more shallow or intentionally made deeper by diffusing the dopant in an ambient that alters the diffusing in silicon. Two examples of such ambients are ones that includes oxygen or ammonia. For instance, if the diffusion takes place in an ambient of 10% oxygen and 90% nitrogen the junction depth is reduced by approximately 20% compared to diffusion in an ambient of 100% nitrogen. In general, the oxygen atoms displace silicon atoms in the silicon lattice thereby slowing the diffusion of the boron in silicon. Other annealing ambients or compounds that provide this function may be used.

Well-known processing may be used to complete the fabrication of the integrated circuit shown in Figure 6. The glass layers 16 and 35 to the extent remaining as shown in Figure 6 may remain in place for the remainder of the processing and may stay in the completed integrated circuit. Glass layer 35 may be removed to facilitate a subsequent selective TiSi or $CoSi_2$ layer on gates 11 and 12 and regions 41 and 45.

Figure 8 shows one additional processing step which may be used prior to the deposition of the first glass layer shown in Figure 1. In Figure 8 the substrate of Figure 1 is again shown prior to the deposition of the 2% glass layer. Rather than depositing the glass layer directly onto the silicon substrate 15, an ultra thin layer 60 of silicon dioxide (5-20Å thick) is first formed on the substrate. This layer may be a chemically grown oxide layer. The glass layer is then formed on the silicon dioxide layer. This oxide layer is no thicker than a typical native oxide layer, however, it is intentionally grown to assure its uniformity across the wafer. This is in contrast to a native oxide layer which may not be uniform across the

wafer because of, for example, water drops on the wafer. This oxide strongly affects indiffusion of the boron from the glass. It is more difficult to reproducibly control the interface properties of bare silicon or silicon with a non-controlled growth of a native oxide. The ultra thin oxide layer provides a uniform interface and thereby assures more predictable diffusion of the boron into the substrate. As mentioned earlier, this oxide is also formed prior to the deposition of the second glass layer.

In Figure 9 another processing step which may be used to modulate the diffusion rate of the indiffused boron dopant is shown. In Figure 9, prior to the formation of the glass layer on the substrate the surface of the substrate is amorphized (essentially damaged) by the implantation of a heavy neutral species such as silicon or implanted with a neutral species such as carbon which alters the boron diffusing in silicon. Other heavy or neutral atoms may be used such as arsenic, antimony, indium, nitrogen, fluorine, etc. While in Figure 9 this implantation is shown prior to the formation of the glass layer, the implantation may occur after the formation of the glass layer, that is through the glass layer. The damaging of the substrate surface or presence of neutral species in the substrate surface in this manner can be used to slow the rate of diffusion creating a shallower junction. Silicon damage above 3e14 dose reduces the boron diffusion.

The various techniques for reducing the diffusion or controlling it, such as the growing of the 5-20Å of silicon dioxide, the damaging of the upper surface of the substrate, implantation of a neutral species of diffusion in the ambient of oxygen, etc., and the densification of the glass layers prior to their patterning may be used in combination or alone for improving the reliability and performance of the resultant transistors.

The result of the processing described above is a source and drain region for the p-type transistor having a tip region 40 adjacent to the gate (from the dopant diffused into the substrate from the 2% BSG layer 16) and a more highly doped main portion of the source and drain regions 41 spaced apart from the gate (from the dopant diffused from the 6% BSG layer 35). For the described embodiment the p-type tip region has a dopant concentration of $1\text{-}5\times10^{19}cm^{-3}$ while the main portion of the

source and drain region has a dopant concentration of 2-5x$10^{20}cm^{-3}$. This results directly from the 2% and 6% BSG. Other concentrations of dopants in the glass may be used. For example, layer 16 may have a dopant concentration between 1 to 4% and layer 35 may have a dopant concentration between 6 to 12%.

The ultra-shallow p^+ regions formed with the described invention, as illustrated in the figures has shown to provide substantial improvement over prior art fabrication where the p-channel source and drain regions are formed with a tip implant in alignment with the gate followed by implantation of the main portion of source and drain regions in alignment with a spacer. Transistors made with the low damage doped source and drain regions of the present invention have shown in one benchmark to have a 25% improved gate delay when operated at 1.8v even when compared to a prior art transistor operated at 2.5v.

With the present invention as described above, two masking steps are saved when compared to the prior art technique of forming the p-channel device through two implantation steps, one for the tip implant and the other for the main portion of the source and drain regions. Note that with the present invention, the two masking steps used to expose those areas of the substrate which are doped with the n-type dopant for the n-channel transistor source and drain region are also used to etch the BSG layers 16 and 35. In the prior art, two additional masking steps are needed to protect the n-channel device when the p-channel device are implanted.

As shown in Figure 5, the glass layer 35 is etched in alignment with the photoresist members 40 prior to the implantation illustrated by lines 41. It may be desirable in some processes to leave the 6% BSG layer in place. The second ion implantation step used to form the N+ source and drain regions for the n-channel transistor is then done through this glass layer. The counter doping effect of the boron dopant in the n-type source and drain regions in general will not present a problem. The arsenic dopant level of the source and drain region for the n-channel transistor is high and consequently, not significantly affected by the introduction of the boron atoms. Leaving layer 35 in place saves the step

used to remove this layer from the areas not protected by the photoresist members.

While in the above description, the p-channel transistor is shown fabricated with the present invention and the n-channel transistor is fabricated using conventional ion implantation, the n-channel transistor may likewise be fabricated using one or two layers of glass phosphorous or arsenic doped glass.

While in the above-described process the dopant for the p-channel transistor was obtained from a glass, specifically BSG, other materials may be used as a source of the dopant such as polysilicon or germanium-silicon.

Figure 7 illustrates alternate processing where a single glass layer doped with an n-type dopant is used. For this processing following the etching of the glass layer 35, an additional glass layer 50 doped with the n-type dopant (e.g., 6% PSG) is formed as shown in Figure 7. (The glass layer 50 is formed over the structure shown in Figure 5 without the photoresist layer 40). During the driving step used to dope the source/drain and gate of the p-channel transistor the n-channel transistor is simultaneously formed. Dopant from layer 50 forms the main source/drain regions of the n-channel transistor. Note the dopant from layer 50 does not diffuse into the layer 35. This dopant also diffused under the spacers on gate 12 to form more lightly doped tip regions for the n-channel transistor. At the same time, the gate 12 is doped with the n-type dopant from layer 50.

Note that the glass layer 16 need not be used to form the p-channel transistor. That is, as in the case of the n-channel transistor described in conjunction with Figure 7, the dopant may be driving under the spacer from the 6% glass layer to form the tip source/drain regions. This permits the doping of source/drain for both n-channel and p-channel transistors with a single masking step.

Thus, an improved process and structure for providing doping for a source and drain region has been described which employs two layers with different doping concentrations to permit simultaneously doping of a

lightly doped tip regions and more heavily doped main portions of source and drain regions. Ultra shallow source and drain regions are obtained with improved short channel properties.

CLAIM

1. In the fabrication of a transistor on a substrate, an improved method comprising the steps of:

forming a source of dopant source having a more lightly doped region adjacent to a gate and a more heavily doped region spaced-apart from the gate; and

diffusing the dopant from the source of dopant into the substrate in an ambient that changes the rate of the diffusion.

2. The method defined by clam 1 wherein the ambient includes oxygen.

3. The method defined by claim 1 wherein the ambient includes ammonia.

4. A method for doping a source and drain region for a field-effect transistor in a substrate region doped with a first conductivity type dopant comprising the steps of:

forming a gate insulated from the substrate region;

forming a first solid source of dopant of a second conductivity type dopant laterally adjacent to opposite sides of the gate in proximity to the substrate such that the second conductivity type dopant can be diffused from the first source of dopant into the substrate;

forming a second solid source of dopant of the second conductivity type dopant laterally spaced apart from opposite sides of the gate in proximity to the substrate such that the second conductivity type dopant can be diffused from the second solid source of dopant into the substrate, the second source of dopant being more heavily doped with the second conductivity type dopant than the first dopant source; and

diffusing the second conductivity type dopant from the first and second sources of dopant to form source and drain regions for the transistor in an ambient that reduces the extent of the diffusion.

5. The method defined by claim 4 wherein the first source of dopant comprises a first glass layer.

6. The method defined by claim 5 wherein the second source of dopant comprises a second glass layer.

7. The method defined by clam 6 wherein the ambient includes oxygen.

8. The method defined by claim 6 wherein the ambient includes ammonia.

9. The method defined by claim 8 wherein spacers are formed on the opposite sides of the gate after the forming of the first source of dopant but before the forming of the second source of dopant source.

10. In the fabrication of a transistor on a substrate, an improved method comprising the steps of:

forming a doped glass layer on the substrate;

annealing the glass layer;

patterning the glass layer using a photoresist; and,

diffusing the dopant from the glass layer into the substrate so as to form at least portions of source and drain regions for the transistor.

11. The method defined by claim 10 wherein the annealing occurs between approximately 650º to 800ºC.

12. The method defined by claim 11 wherein the diffusing step occurs at approximately 1000ºC or above.

13. A method for forming a field-effect transistor on a substrate region doped with a first conductivity type dopant comprising the steps of:

forming a gate on the substrate;

forming a first glass layer containing a second conductivity type dopant over the substrate including over the gate;

annealing the first glass layer;

forming spacers on opposite sides of the gate over the first glass layer;

forming a second glass layer containing the second conductivity type dopant over the substrate including over the gate spacers and first glass layer, the second glass layer containing a higher concentration of the second conductivity type dopant than the first glass layer;

annealing the second glass layer;

patterning the second glass layer; and,

diffusing the second conductivity type dopant from the first and second glass layers into the substrate to form source and drain regions for the field-effect transistors.

14. The method defined by claim 13 wherein the annealing of the first the second glass layer each occurs at approximately between 650° to 800°C.

15. In the fabrication of a transistor on a substrate where at least a portion of a source and drain region for the transistor are formed by shaggy

a dopant from a glass layer, an improved process comprising:

damaging the surface of the substrate;

forming the glass layer over the damaged surface of the substrate or a substrate with implanted neutral species; and,

indiffusing the dopant from the glass layer through the damaged surface or neutral species region to form the portion of the source and drain region.

16. The process defined by claim 15 wherein the step of damaging the substrate comprises ion implantation.

17. The process defined by claim 15 wherein the step of impregnating the substrate with a neutral species involves ion implantation.

18. The process defined by claim 16 wherein the step of ion implantation comprises implanting silicon.

19. The process defined by claim 17 wherein the step of ion implantation comprises implanting carbon.

20. In the fabrication of a transistor on a substrate where at least a portion of a source and drain region for the transistor are formed by indiffusing a dopant from a glass layer, an improved process comprising:

growing an oxide layer on the surface of the substrate;

forming the glass layer oxide layer ;

indiffusing the dopant from the glass layer through the oxide layer to form the portion of the source and drain regions.

21. The process defined by claim 20 wherein the step of growing an oxide on the substrate comprises growing an oxide of approximately between 5 to 20Å.

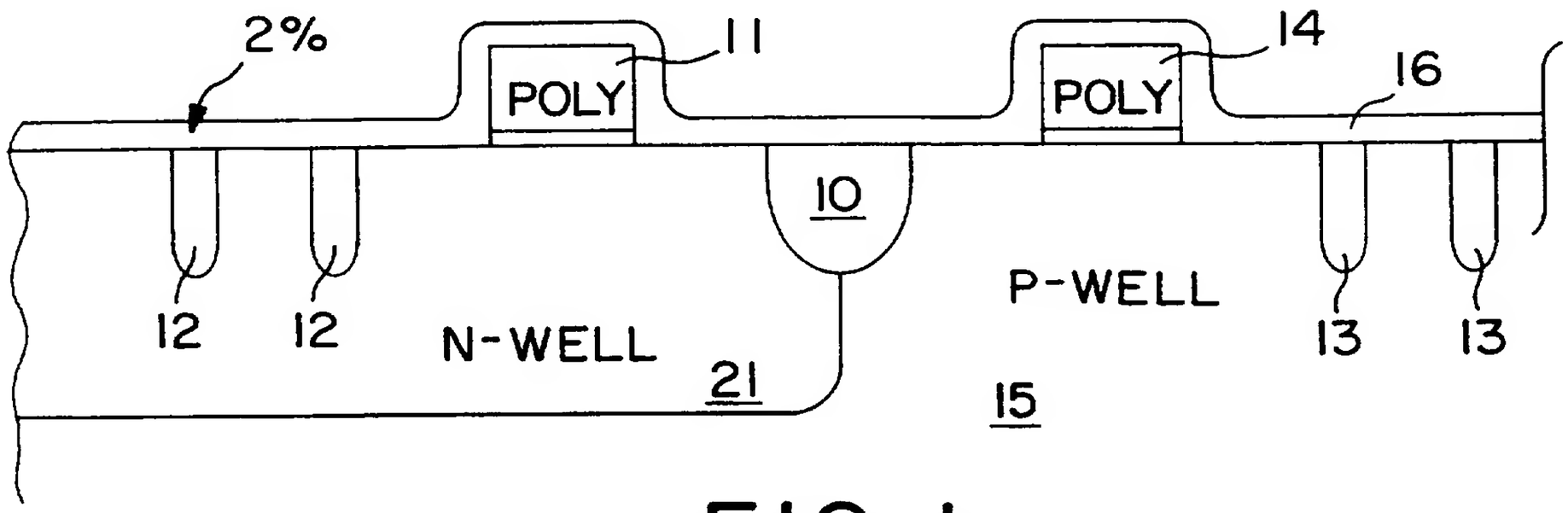

2%
11
POLY
14
POLY
16
10
12
12
N-WELL
21
P-WELL
13
13
15

FIG. 1

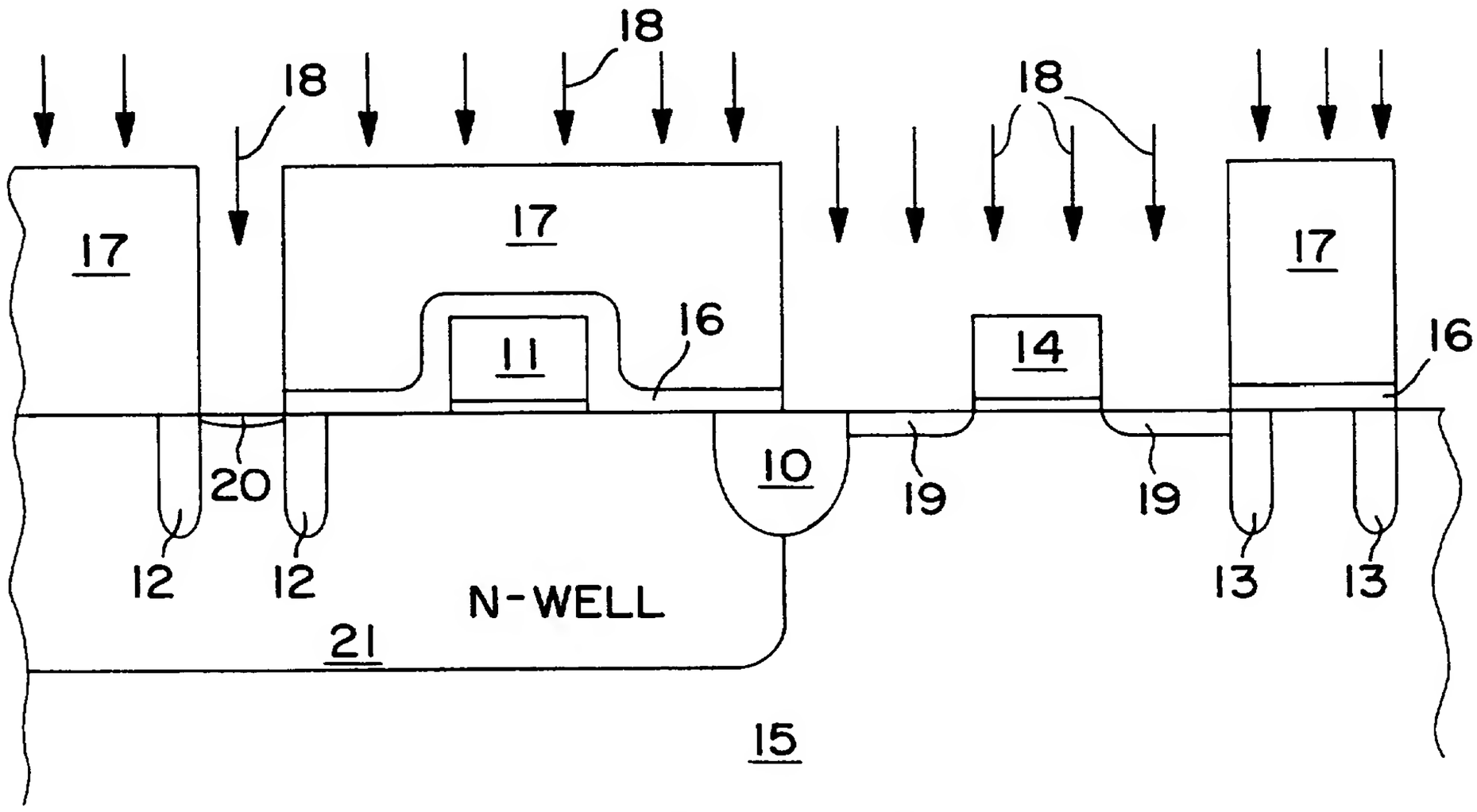
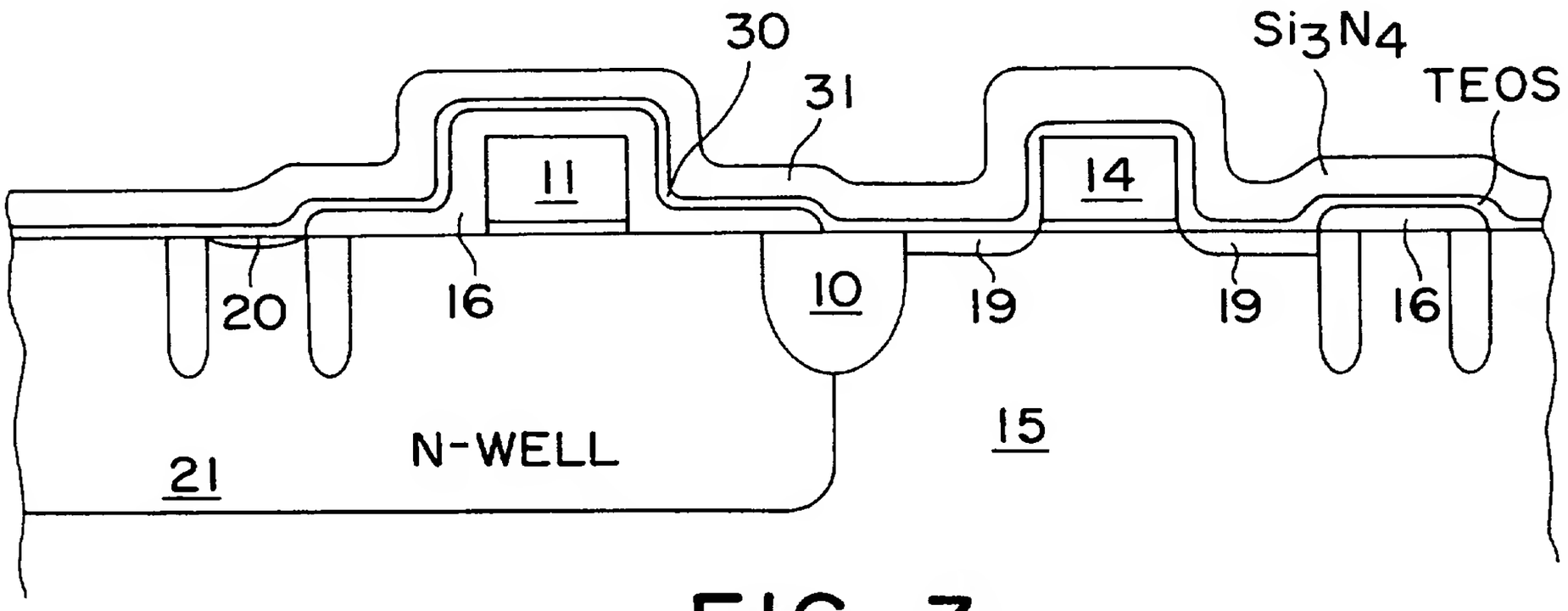

18
18
18
17
17
17
16
11
14
16
10
20
19
19
12
12
N-WELL
21
13
13
15

FIG. 2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31
Si3N4
TEOS
11
14
20
16
10
19
19
16
N-WELL
21
15

FIG. 3

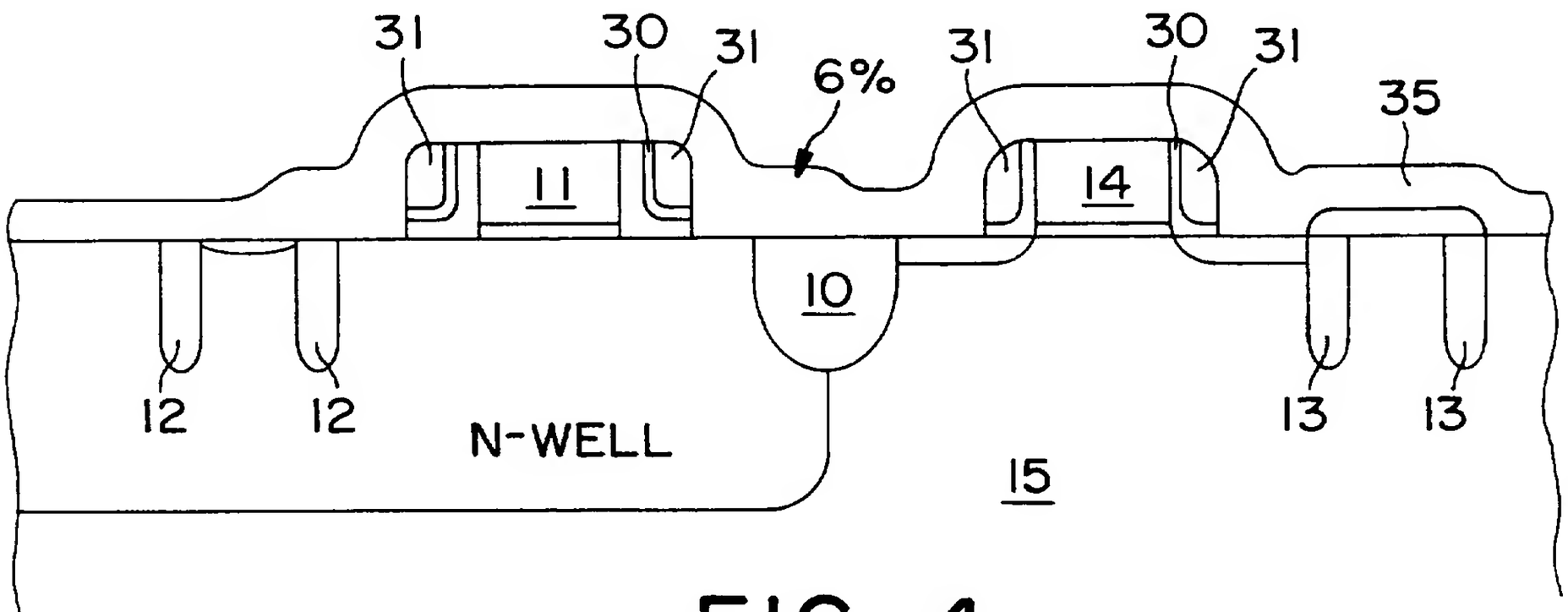
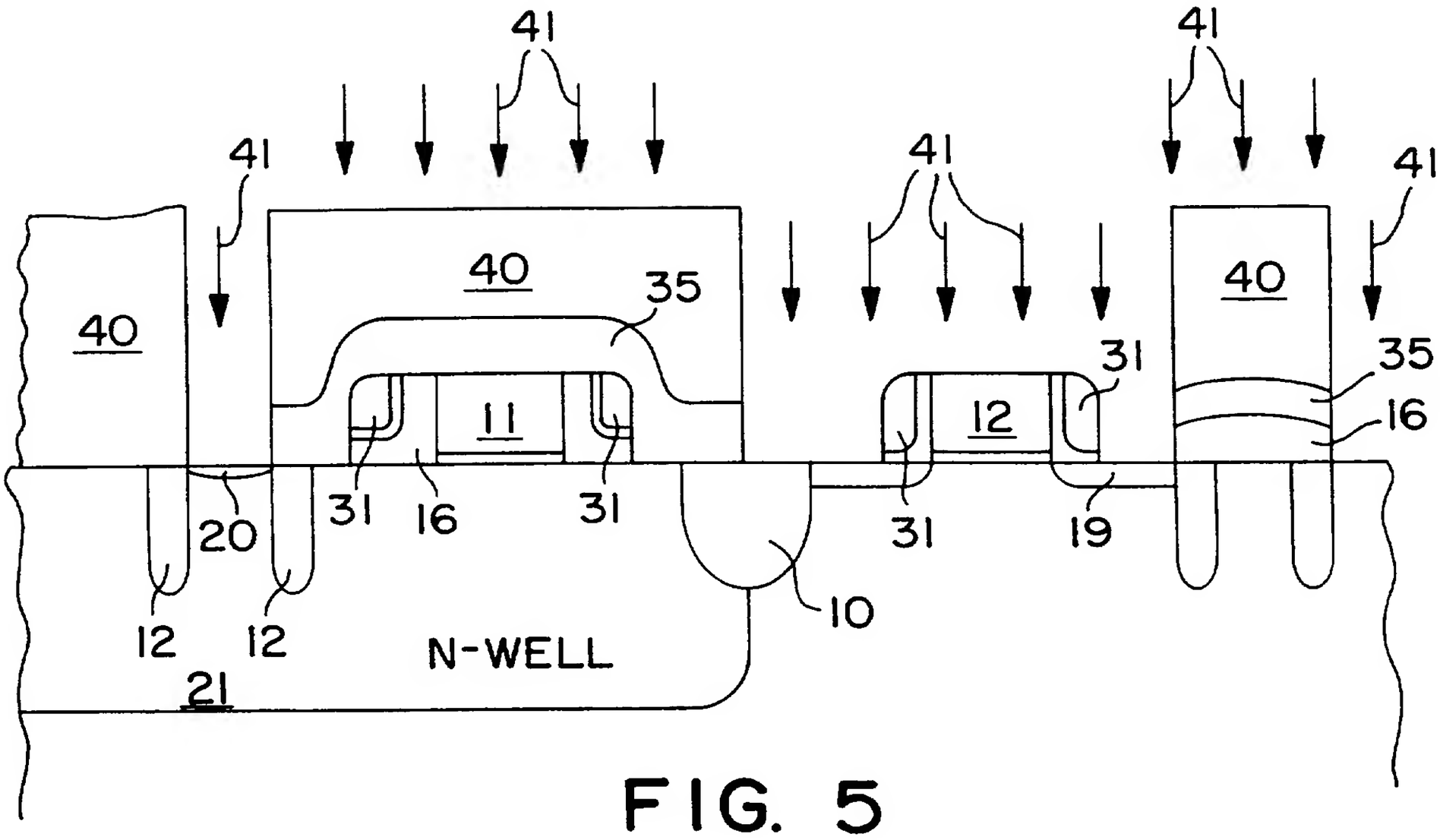

31
30
31
6%
31
30
31
35
11
14
10
12
12
13
13
N-WELL
15

FIG. 4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41
41
41
40
40
35
31
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16
11
12
31
16
31
31
19
20
12
12
N-WELL
10
21

FIG. 5

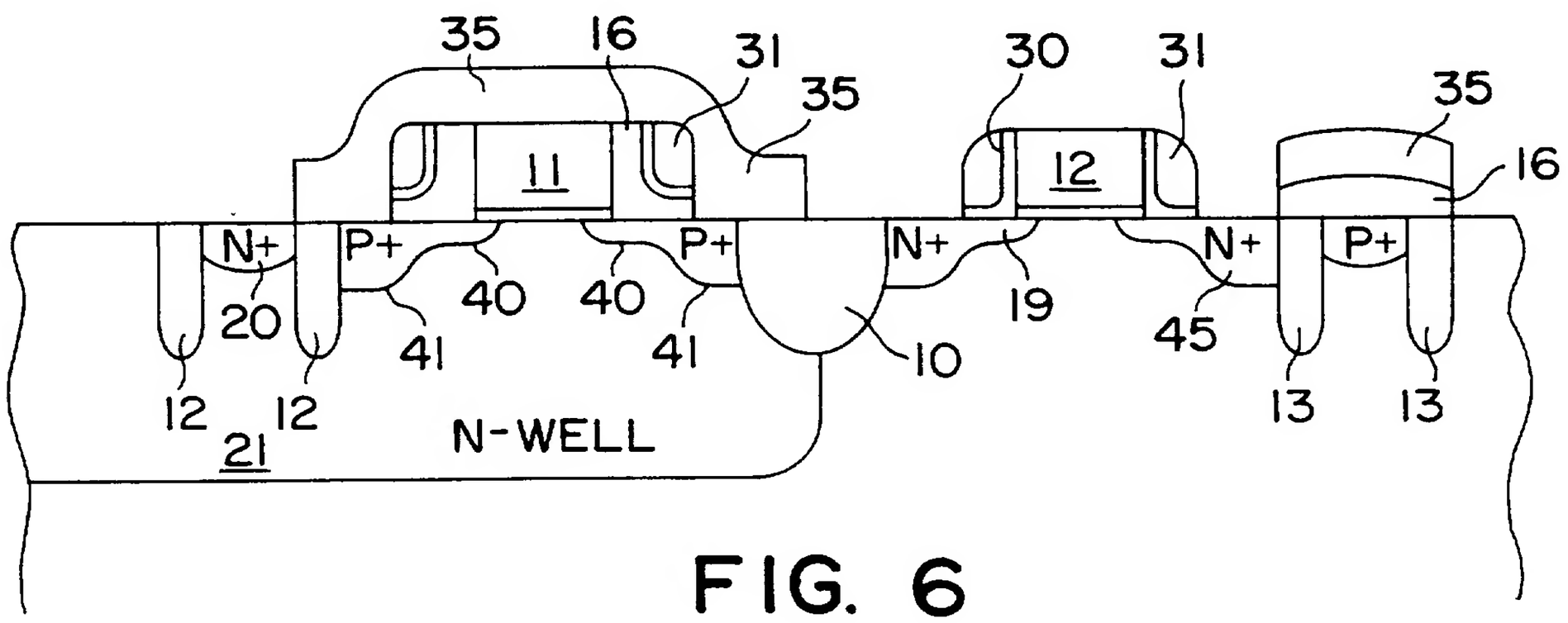
35
16
31
35
30
31
35
16
11
12
N+
P+
P+
N+
N+
P+
20
40
40
19
45
41
41
10
12
12
13
13
21
N-WELL

FIG. 6

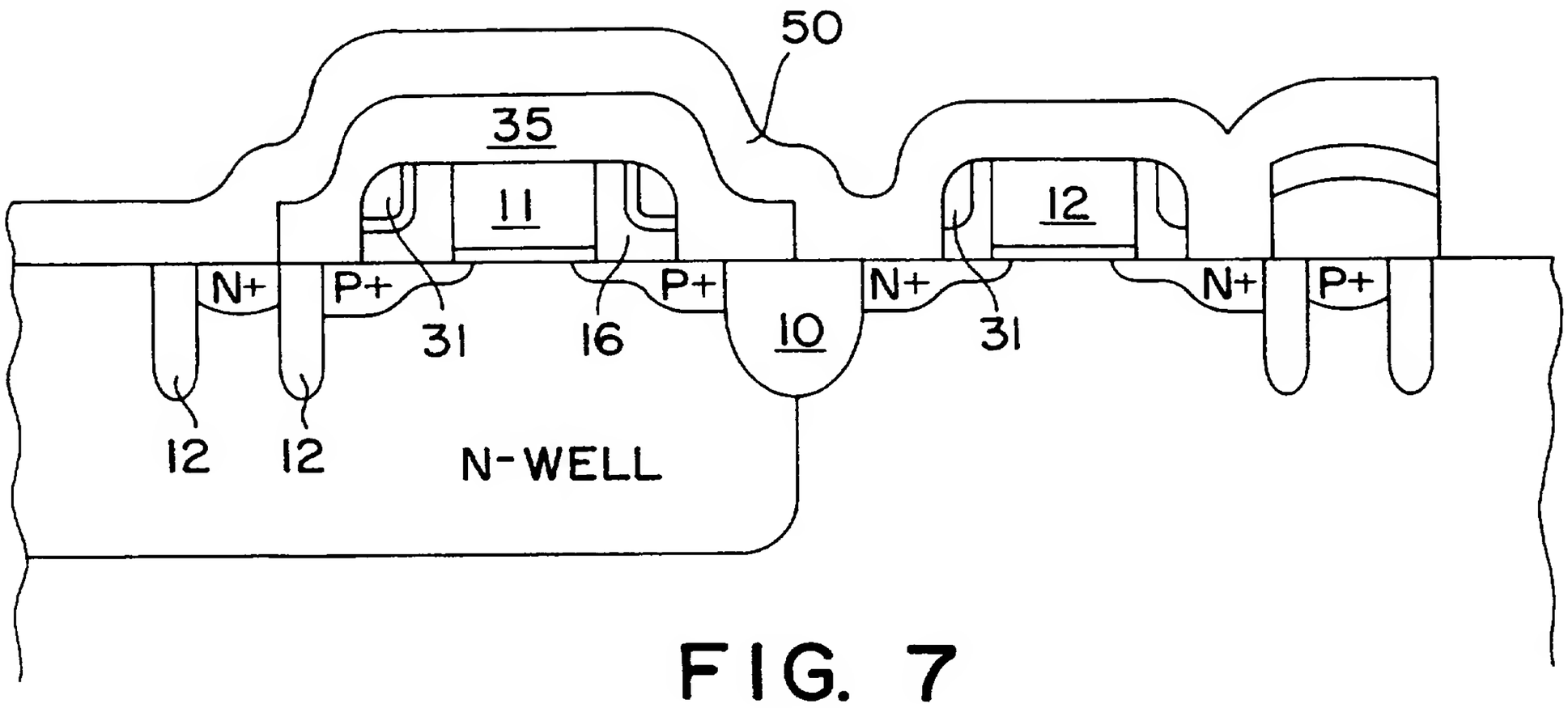

FIG. 7

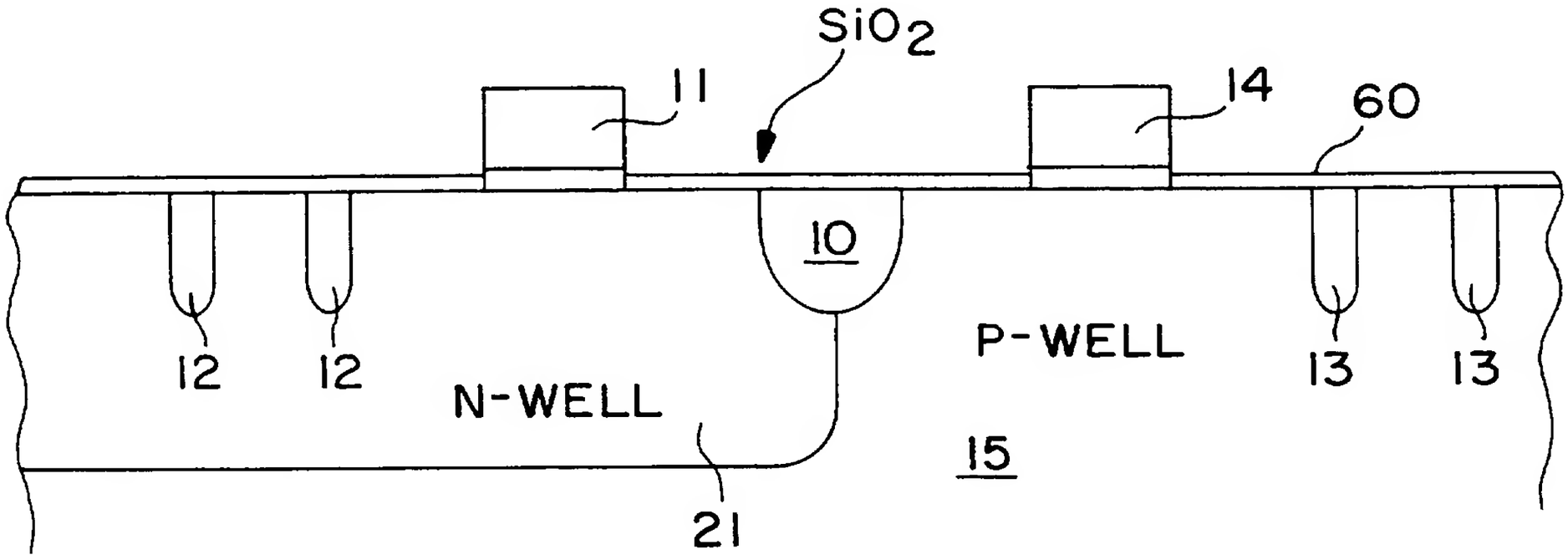
SiO2
11
14
60
10
12
12
P-WELL
13
13
N-WELL
15
21

FIG. 8

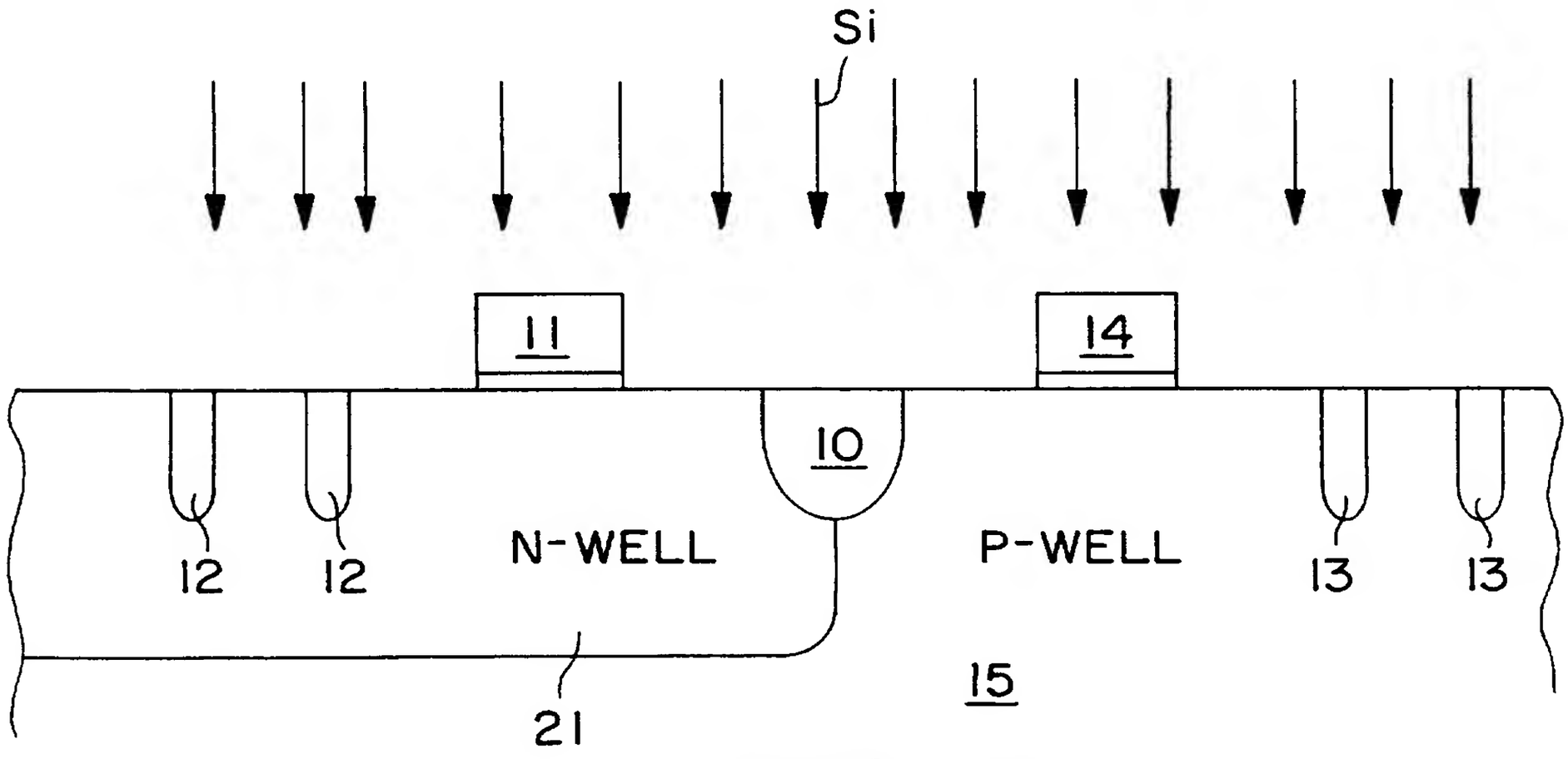
Si
11
14
10
12
12
N-WELL
P-WELL
13
13
15
21

FIG. 9

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US96/16002

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) :H01L 21/385, 21/8232
US CL : 437/34, 44, 164

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 437/24, 40SW, 41SW, 34, 44, 57, 160, 164

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

Please See Extra Sheet.

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X --- Y	US 4,204,894 A (Komeda et al) 27 May 1980, col. 3, line 35 through col. 8, line 59, Figs. 2A-6, especially col. 4, lines 12-15.	1,2,4-7 ------- 3,8-21
X,P --- Y	US 5,518,945 A (Bracchitta et al) 21 May 1996, col. 2, line through col. 5, line 25, Figs. 2-6, especially col. 5, lines 5-13, col. 3, lines 30-40.	1,4-6,20 ------- 2,3,7-19,21
Y	US 5,348,900 A (Ayukawa et al) 20 September 1994, col. 2, line 62 through col. 3, line 8.	2-3,7-9
Y	US 4,102,715 A (Kambara et al) 25 July 1978, col. 5, lines 5-60.	3,8-9

[X] Further documents are listed in the continuation of Box C. [ ] See patent family annex.

* Special categories of cited documents:

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"E" earlier document published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
06 DECEMBER 1996	08 JAN 1997

Name and mailing address of the ISA/US	Authorized officer
Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231	MICHAEL TRINH
Facsimile No. (703) 305-3230	Telephone No. (703) 308-0661

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/US96/16002

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 3,600,797 A (Bower et al) 24 August 1971, col 3, lines 57-66.	16-19
Y	US 5,094,984 A (Liu et al) 10 March 1992, cols 3-11, especially col. 2, lines 30-40.	10-14
X -- Y	JP 62-266829 A (Hasegawa) 19 November 1987, English Abstract and figs. 1a-e.	15-18 --- 19
Y	Kenneth Mason Publication Ltd, England, Self-Aligning Dopinng Process Using Oxidized Dopants, Reseach Disclosure, June 1988, Number 290, 29097	21

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US96/16002

B. FIELDS SEARCHED
Electronic data bases consulted (Name of data base and where practicable terms used):

Databases: APS
Search terms: implant?, si or carbon, BSG or BPSG or PSG or PBSG or doped glass, heat? or anneal?, oxygen or ammonia, densif?, source#